Attorney's Docket No. PD-00W014

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

ALLISON et al.

Serial No. 09/607,604

Filed: 06/30/2000

For: MULTI-BIT PHASE SHIFTERS USING MEM RF SWITCHES

Art Unit: 2817

Examiner: Lee, B.

Date: August 1, 2003

Approved for Entry

RESPONSE TO FINAL REJECTION

Commissioner for Patents
P.O. Box 1450
Arlington, VA

Dear Sir:

In response to the Office Action mailed June 5, 2003, kindly amend the application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-4 (canceled)

5. (Previously Amended) The array of Claim 27 wherein said MEM switches are single-pole-single-throw (SPST) switches including an armature for opening and closing the RF signal path through the switch, and a control signal path, and wherein the control signals are isolated from the RF signal path.

Claims 6-12 (canceled)

13. (Previously Amended) The circuit of Claim 31, wherein said first and second MEM switch circuits provide MPMT switching functions.

14. (Previously Amended) The circuit of Claim 31, wherein said MEM switches are metal-metal contact RF MEMS series switches.

Claims 15-20 (canceled)

21. (Previously Amended) The circuit of Claim 27, wherein said first and second MEM switch circuits provide MPMT (multiple-pole-multiple-throw) switching functions.

Claims 22-25 (canceled)

26. (Cancel)

27. (Currently Amended) An electronically scanned array, comprising:

a linear array of radiating elements;

an array of reflection phase shifters coupled to the radiating elements;

an RF manifold including a plurality of phase shifter ports respectively coupled to a corresponding phase shifter RF port and an RF port; and

a beam steering controller for providing phase shift control signals to the phase shifters to control the phase shift setting of the array of the phase shifters;

and wherein said phase shifters each include:

a plurality of micro-electro-mechanical ("MEM") switches responsive to said control signals to select one of a discrete number of phase shift settings for the respective phase shifter;

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports, and first and second reactance circuits respectively coupled to the in-phase and

quadrature ports by first and second MEM switch circuits, said first and second reactance circuits each comprising a plurality of susceptances connected in parallel for terminating said in-phase or quadrature port, and wherein said first and second MEM switch circuits select at least one of said plurality of susceptances connected in parallel for each of said first and second reactance circuits to select a phase shift setting, and wherein ~~each of~~ said plurality of susceptances can be selected ~~individually and~~ in parallel combinations.

28. (Previously Presented) The array of Claim 27, wherein said first and second MEM switch circuits each comprise first, second and third MEM switches each terminated respectively in a first, second or third one of said plurality of susceptances.

29. (Currently Amended) The array of Claim 28, wherein said plurality of susceptances can be switched ~~individually and in parallel combinations~~ to provide at least eight different discrete phase settings.

Claim 30 (canceled)

31. (Currently Amended) An RF reflection phase shifter circuit, comprising:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the phase shifter circuit to RF signals passed between the first and second RF ports, said circuits connected to provide a single-pole-multiple-throw (SPMT) or multiple-pole-multiple-throw (MPMT) switch function;

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable ~~individually and~~ in parallel combinations to select different phase shift values.

Claim 32 (canceled)

33. (Currently Amended) A multi-section RF phase shifter circuit, comprising:

a plurality of reflection phase shift sections connected in series to provide a discrete set of selectable phase shifts to RF signals passed through the circuit, and wherein each reflection phase shift section includes:

a coupler device having first and second RF I/O ports, and in-phase and quadrature ports;

a switch circuit comprising a plurality of single-pole-single-throw (SPST) micro-electro-mechanical ("MEM") switches responsive to control signals, said switch circuit arranged to select one of a plurality of discrete phase shift values introduced by the phase shifter circuit to RF signals passed between the first and second RF ports;

said MEM switch circuit including first and second reactance switch circuits selectively coupling first and second termination reactance circuits respectively to the in-phase and quadrature ports, each said reactance circuit including a plurality of selectable reactance values connected in parallel which are selectable ~~individually and~~ in parallel combinations to select different phase shift values.

34. (Previously Presented) The array of Claim 27, wherein the respective plurality of susceptances comprising said first and second reactance circuits define pairs of equal susceptances which are switched in tandem to provide symmetrical operation.

35. (Previously Presented) The circuit of Claim 31, wherein the respective plurality of selectable reactance values connected in parallel for the first and second termination reactance circuits define pairs of equal reactance values which are switched in tandem to provide symmetrical operation.

36. (Previously Presented) The circuit of Claim 33, wherein the respective plurality of selectable reactance values connected in parallel for the first and second termination reactance circuits define pairs of equal reactance values which are switched in tandem to provide symmetrical operation.